

PATENT
4444-0120P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: LEE, Chin Conf.:
Appl. No.: NEW Group:
Filed: July 17, 2003 Examiner:
For: MEMORY MODELING CIRCUIT WITH FAULT
TOLERATION

L E T T E R

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 17, 2003

Sir:

Under the provisions of 35 U.S.C. § 119 and 37 C.F.R. § 1.55(a), the applicant(s) hereby claim(s) the right of priority based on the following application(s):

<u>Country</u>	<u>Application No.</u>	<u>Filed</u>
TAIWAN, R.O.C.	091134866	November 29, 2002

A certified copy of the above-noted application(s) is(are) attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By 
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KM/sll
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Attachment(s)

(Rev. 04/29/03)